

# TMC2360P7CKL

## Video Output Processor Evaluation Kit

### Introduction

A flicker-free PC-to-TV encoding is demonstrated on the TMC2360P7CKL evaluation board. Mounted on the TMC2360P7CKL board is a TMC2360KLC part (80-pin MQFP). With an external VGA source, either +5 or +9 volt power, and a TV monitor, TMC2360 performance can be evaluated.

Although the TMC2360 can operate with a minimum of external components, included on the board are a number of options such as alternate clocks, a microprocessor interface and x/sinx filters that allow various configuration options to be explored.

### Kit Contents

Within the evaluation kit are seven items:

- TMC2360 MQFP demo board
- TMC236X Software
- Power brick
- S-video cable (Y/C)
- Composite video cable (RCA)
- VGA cable
- Instructions document

### Quick Setup for NTSC

1. Install jumpers JP13 (if oscillator), 14 (if crystal), 20 and 21.

2. Set DIP switches CVIDEN → OFF, SVIDEN → OFF,  $\overline{\text{PWRDN}}$  → OFF, TVSTD0 → OFF and all other DIP switches → ON.
3. Connect a 640\*480/60 Hz VGA source to J7.
4. Connect J4 to VGA monitor. (optional)
5. Connect either RCA-type video cable from connector J1 or S-video cable from J3 to TV monitor.
6. Connect 5±0.2 Volt/ 0.5 amp DC source to connector J6 (see PWB silk-screen for polarity) or 9 volt/0.5 amp DC supply to connector J8.
7. Observe images on VGA monitor and TV monitor.

### Quick Setup for PAL

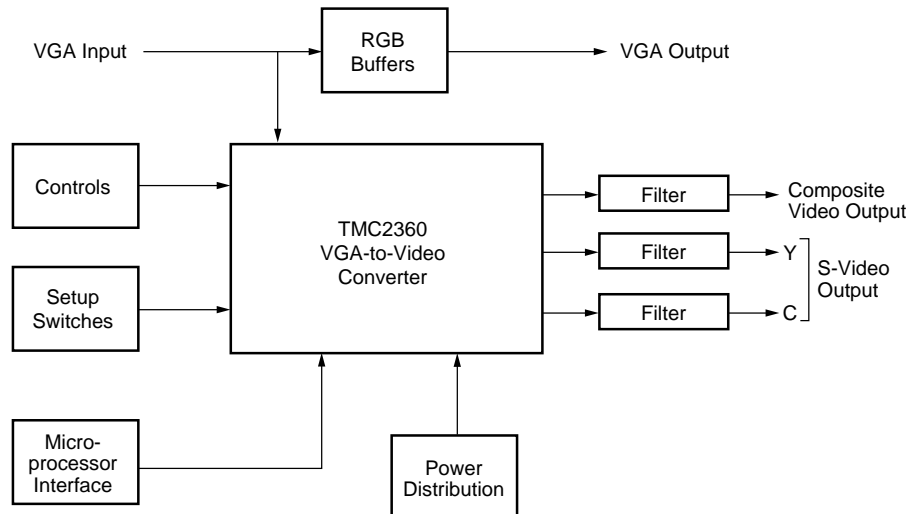
Repeat *Quick Setup for NTSC* except:

1. Set VGA source to 640\*480/50 Hz.
2. Set DIP switch TVSTD1 → OFF and TVSTD0 → ON

### Operational Information

In its basic configuration, the TMC2360P7CKL Evaluation Board is intended to demonstrate how the TMC2360 can be used to convert VGA video to TV video with a minimum

### Block Diagram



number of external components. Extra components are included on the board to permit evaluation of alternate configurations such as external clocks and the microprocessor interface.

### Basic Configuration

In this configuration, install the following jumpers (see Table 1):

- JP13 (if oscillator)
- JP14 (if crystal)
- JP15 (if crystal)
- JP20
- JP21

Note that JP1, JP2, JP3, JP9, JP10, JP11 are pre-installed at the factory.

In addition, remove the following jumpers:

- JP4
- JP5
- JP6
- JP7
- JP8
- JP12
- JP13 (if crystal)
- JP14 (if oscillator)
- JP15 (if oscillator)

Note that JP16, JP17, JP18 are open circuit from factory.

All switch and push-button functions are available. Either of two power sources may be used. With JP19 removed, +5 volt power may be connected directly to connector J6. Alternatively, with JP19 installed, 9 volt power may be connected via the 2.1 mm jack, J8.

Image attributes may be controlled by three switches:

- PHASE optimizes VGA data sampling by inverting the internal ADCLK of the TMC2360.
- BLANK blanks the image to the color set by BLUE.
- BLUE = OFF sets the blank color to blue. BLUE = ON sets the blank color to black.

Switches TVSTD0 and TVSTD1 allow one of four output standards to be selected:

TVSTD <sub>1-0</sub>	Television Standard
00	NTSC-EIAJ
01	NTSC
10	PAL/B, G, I
11	PAL/M

Switch PAL800 → OFF sets timing and clocks for conversion of 50Hz 800x600 pixel VGA images.

Supplied with the board is a 27 MHz oscillator, Y1 or a 27 MHz crystal Y2. JP13 or JP14 and JP15 must be installed to select the correct source. With JP13, 14, and 15 removed and JP12 installed, the TMC2360 clock may be supplied from an external 27 MHz source connected to J5.

Power Management may be implemented through three switches:

- CVIDEN = OFF enables the composite video output.
- SVIDEN = OFF enables the S-Video output.
- PWRDN = OFF powers down the TMC2360 into a sleep mode.

Software control through VGA sync signals is enabled by two switches:

- DPMS = OFF enables display power management. Missing HSYNC or VSYNC signals will blank the screen and/or power down the TMC2360. (see data sheet)
- VSCOM = OFF enables vertical sync communications. The number of HSYNC pulses per vertical sync period will set the TV standard and the filter mode. (see data sheet)

### Optional Configurations

Optional configurations are programmed by installing jumpers (see Table 1) and by use of alternate connections (see Table 2).

JP12, 13, 14 and 15, allow the 27 MHz clock to be sourced from either a board mounted oscillator or crystal or an external clock.

To access the VGA registers through the microprocessor port, the MPEN switch must be set OFF. For microprocessor programming information refer to the TMC2360 data sheet. Contact Raytheon Electronics for a schematic and PAL equations for a simple programming tool.

For probing without an external TV monitor connected, JP4, 6 and 7 add 75 Ω loads to the filter outputs.

Connectors J6 and J8 allow connection of either 9 volt DC or 5 volt DC power.

J1 and J3 allow connection of either composite or S-Video (Y/C) to a TV monitor.

**Table 1. Jumpers**

<b>Jumper</b>	<b>Function (when installed)</b>
JP1	Connects composite video filter output to J1
JP2	Connects luminance video filter output to J3
JP3	Connects chrominance video filter output to J3
JP4	Adds 75Ω load to Composite Video Filter Output
JP5	Adds 75Ω load to Luminance Video Filter Output
JP6	Adds 75Ω load to Chrominance Video Filter Output
JP7	Enables ADCLK from external phase-locked loop controller
JP8	Enables PXCK from external phase-locked loop controller
JP9	Connects COMP output to composite video filter
JP10	Connects LUMA output to luminance filter for S-video
JP11	Connects CHROMA output to chrominance filter for S-video
JP12	Connects external 27 MHz clock source to XTAL1 input
JP13	Connects 27 MHz Crystal Oscillator to XTAL1 input
JP14	Connects 27 MHz Crystal to XTAL1 input
JP15	Connects 27 MHz Crystal to XTAL2 input
JP16	Bypass L12
JP17	Bypass L13
JP18	Bypass L14
JP19	Connects V <sub>CC</sub> to voltage regulator if external 9 volt DC power is used
JP20	Connect VGA vertical drive, VIN to VGAVS input
JP21	Connect VGA horizontal drive, HIN to VGAHS input

**Table 2. Connectors**

<b>Reference Designator</b>	<b>Function</b>
J1	RCA jack, composite video output
J2	Header for probing XTL27, PXCK and ADCLK clocks
J3	S-video output jack
J4	VGA Out, 15-pin D-Sug
J5	BNC to accept optional external 27 MHz XTAL clock
J6	+5±0.2 Volt DC regulated power input
J7	VGA In, 15-pin D-Sug
J8	Accepts 9±1 volt DC unregulated external power from 2.1 mm. plug
P1	Microprocessor Interface Connector

**Table 3. Switches**

Reference Designator	Acronym	Function	
		ON	OFF
S5	CVIDEN	Disable Video Output	Enable Video Output
	SVIDEN	Disable S-Video Output	Enable S-Video Output
	$\overline{\text{PWRDN}}$	Power down TMC2360	Activate TMC2360
	MPEN	Disable Microprocessor Port	Enable Microprocessor Port
S6	PHASE	Sample clock non-inverted	Image displaced 1/2 pixel left
	TVSTD1	TV Standard bit 1 = L	TV Standard bit 1 = H
	TVSTD0	TV Standard bit 0 = L	TV Standard bit 0 = H
	PAL800	Disable PAL800 mode	Enable PAL800 mode
S7	BLUE	If BLANK switch is OFF, screen blanked to black.	If BLANK switch is OFF, screen blanked to blue.
	BLANK	Video enabled.	Video output blanked
	VSCOM	Disable Vertical Sync Communications	Enable Vertical Sync Communications
	DPMS	Disable Display Power Management	Enable Display Power Management

**Table 4. Pushbuttons**

Reference	Acronym	Function
S1	FIL	Filter Select
S2	POSR	Position Right
S3	POSD	Position Down
S4	RESET	Reset TMC2360

## Theory of Operation

### Power and Grounds

Power may be derived from an external AC/DC module with a 9 volt/700 mA output. Alternatively, if jumper JP19 is removed, a 5 volt/700 mA DC supply may be connected directly to the internal +5 volt bus via connector J8.

A common ground plane is used for both analog and digital signals. But notice that the routing of analog/analog/digital traces over the plane is carefully segregated. Digital and analog traces are not mixed and critical circuits such as PLL filters and crystal oscillator components are separated from other circuits.

Power is also segregated.  $V_{DD}$  to the analog and digital sections is derived from a common source but isolated by ferrite beads. Three other isolated power lines supply the phase locked loops and VGA emitter followers. Note that VDDD and VDDA have a common 22  $\mu\text{F}$  decoupling capacitor to support hefty current surges.

### VGA Interfaces

VGA signals from a 15-pin D-Sub connector, J7 are looped through the board to a VGA output connector, J4. Video signals are buffered by three PNP emitter followers which

elevate the video level from a nominal 0 - 0.7 volt to 0.6 - 1.3 volt.

Horizontal and vertical sync signals from J7 are routed through the TMC2360 to J4. RGB inputs from J7 flow through a low pass filter prior to digitization in the TMC2360.

### User Controls

Three push-buttons control the TMC2360 video output :

- POSR - position right in eight pixel increments reversing extreme right and left positions.
- POSD - position down in eight line increments reversing at extreme down and up positions.
- FIL - Select either one, two or three line vertical filtering trading off smearing of the image against flicker reduction.

One other control is included for engineering evaluation:

- RESET clears all internal registers, setting the vertical filter to the three line mode and positioning the TV image at the center.

### Setup Switches

For most applications, these switches are preset according to the functions defined in the TMC2360 data sheet. Switch Mnemonics are silk-screened on the PWB beside each switch.

### A/D Converter Reference Voltage

Top voltage for the RGB A/D converters,  $V_T$  is supplied by the output  $V_{TOUT}$  of a buffer amplifier with input  $V_{TIN}$  connected to potentiometer VR2. Reference voltage for VR2 is derived from the 1.235 volt  $R_{REF}$  voltage.

Nominally,  $V_{RT}$  is set at 0.85 volts, just above the 0.7 volt VGA video amplitude but can be adjusted lower for attenuated inputs or increased to improve digitization if inputs are amplified.

### D/A Converter Current

Resistance from  $R_{REF}$  to ground sets the video output current. Potentiometer VR1 allows trimming of the output video amplitude.

With a 392  $\Omega$  resistor connected to  $R_{REF}$  the D/A current is 27 mA. (1 volt across 37.5  $\Omega$ ) at 100 IRE units.

### Phase Locked Loop Filters

A/D converter and encoder phase locked loop filters are identical. Each filter is driven by a charge pump (peak current  $I_p$ ) to generate a voltage across the filter network which drives the voltage controlled oscillator. Derivation of the filter parameters without a divide-by-N counter in the feedback loop can be found in Gardner.\*

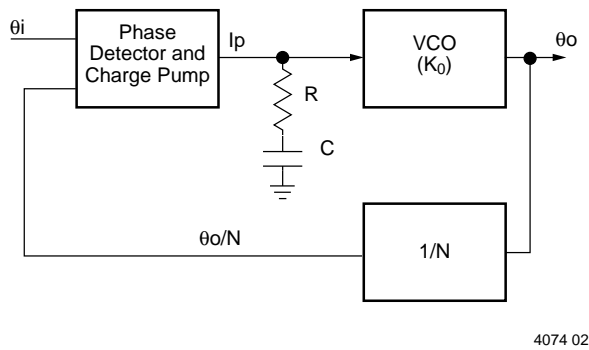


Figure 1. Phase locked Loop Block Diagram

With the divide-by-N counter, the performance is given by:

$$\text{Natural frequency, } \omega_n = \sqrt{(K_0 I_p / 2\pi C N)}$$

$$\text{Damping factor, } \xi = (RC/2) \sqrt{(K_0 I_p / 2\pi C N)}$$

where, for the TMC2360:

$$I_p = 100 \text{ microamps}$$

$$K_0 = 2\pi 10 \text{ Mrad/volt}$$

For  $R = 39 \text{ K}\Omega$  and  $C = 0.1 \mu\text{F}$ :

$$f_n = \omega_n / 2\pi = 563 \text{ Hz}$$

$$\xi = 6.9$$

### 27 MHz Oscillator

A 27 MHz reference signal is supplied to the TMC2360 for the encoder subcarrier synthesizer. This signal may be derived from one of three sources:

- An oscillator connected to XTAL<sub>1</sub>, (JP13),
- A crystal connected across XTAL<sub>1</sub> and XTAL<sub>2</sub>, (JP14,15),
- An external generator connected to J5, (JP13).

Crystal frequency can be trimmed by adding capacitors or changing the 47 pF capacitors shown. Typical pull-in sensitivity for the crystal is 15 ppm/pF.

### Microprocessor Port

TMC2360 VGA registers can be accessed through a microprocessor port which bypasses parameters entered via the ten external setup switches. Each line is pulled low by a 47K resistor. Setting MPEN = H enables the port. Register addresses, bit functions and timing diagrams are included in the TMC2360 data sheet.

### Output Filters

Antialiasing filter design is simplified by operating the three TMC2360 D/A converters in a 2x over-sampling mode. A filter is included in each video output channel to limit the video bandwidth to 10 MHz and provide  $\text{sinc}/x$  correction. With a group delay of 30 nanoseconds across the pass-band, each filter is close to linear phase.

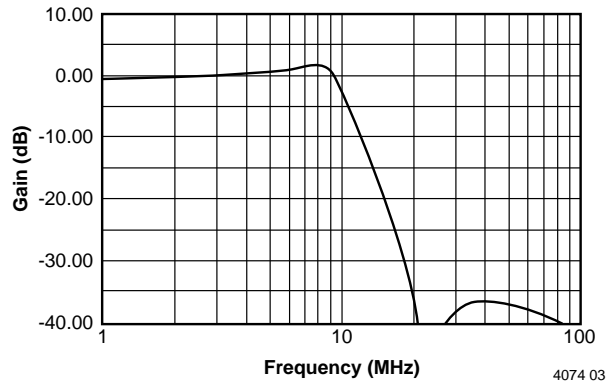


Figure 2. Video Filter Response

\*F. M. Gardner, "Charge-Pump Phase-Lock Loops", *IEEE Trans on Communications*, Vol. COM-28, No. 11, November 1980.

## Printed Wiring Board Layout

Circuits are implemented on a four layer printed wiring board. Interconnects are on layers one and four. Ground is a continuous plane on layer three and power on layer four is split into sections for the digital analog and phase-locked loop sections of the TMC2360. Traces are carefully

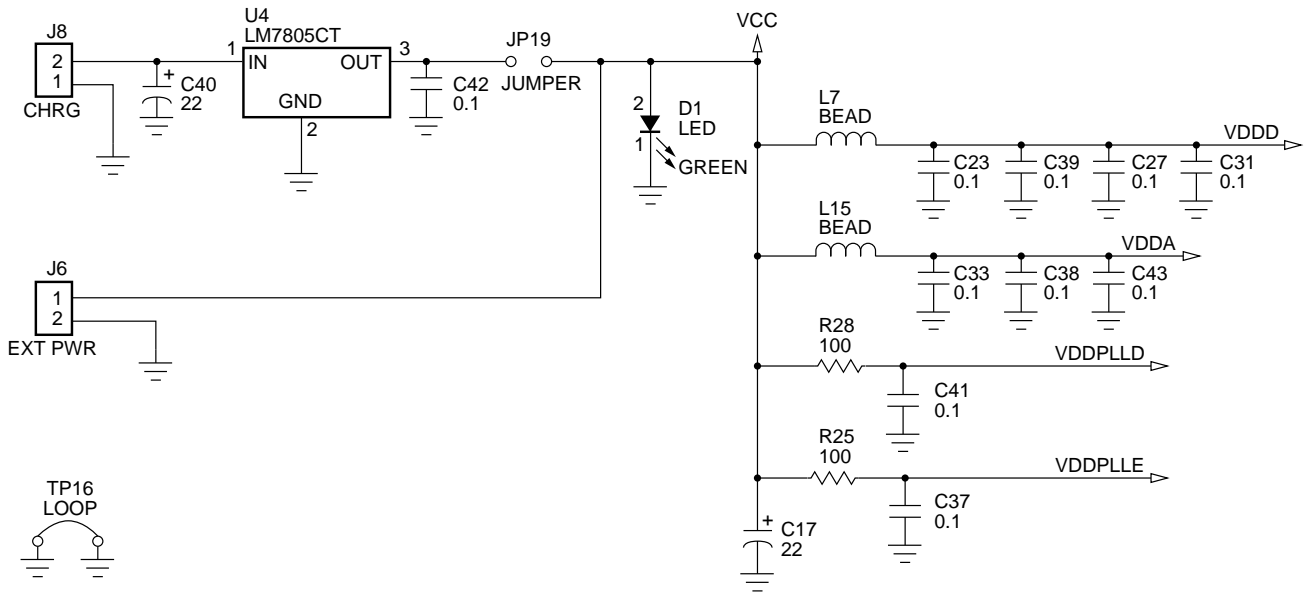
segregated to avoid crosstalk. Each analog connection is run over a continuous ground plane and treated as a transmission line.

For details of layout and interconnection techniques contact Raytheon Electronics for copies of artwork.

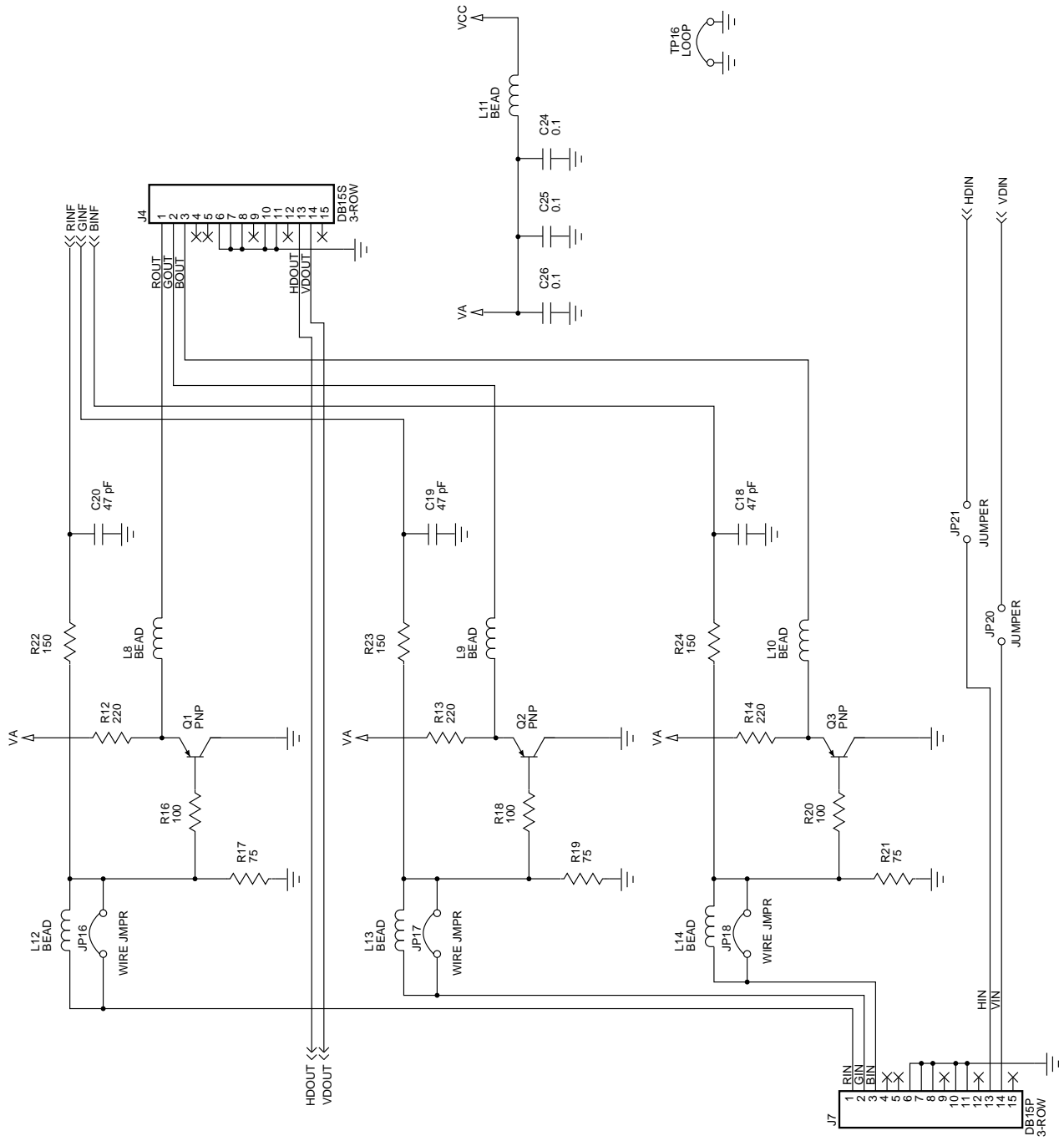
## Schematics

### TMC2360P7CKL Evaluation Board

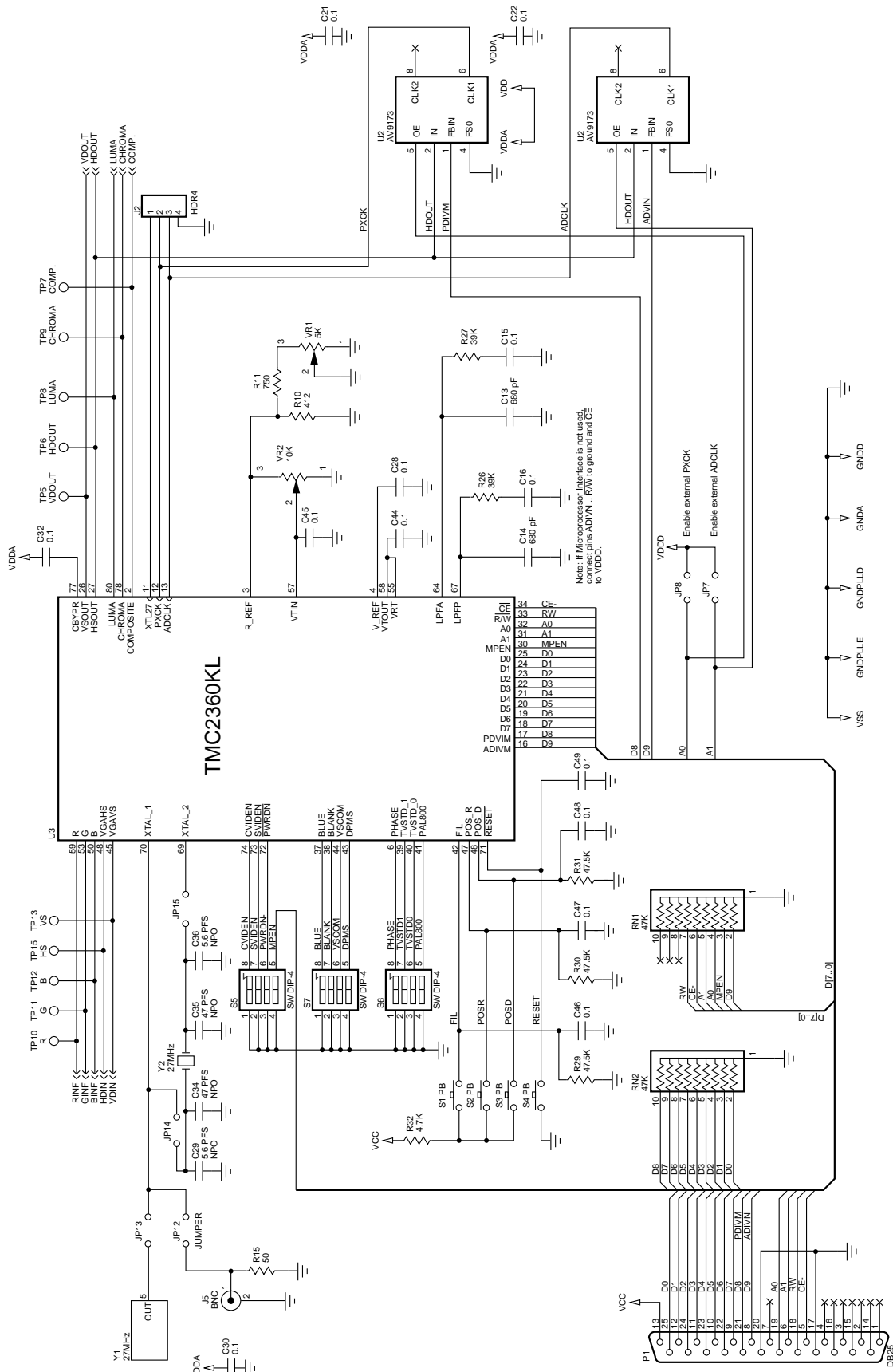
NOTE: LED has integral resistor for 5V operation



# TMC2360P7CKL Evaluation Board

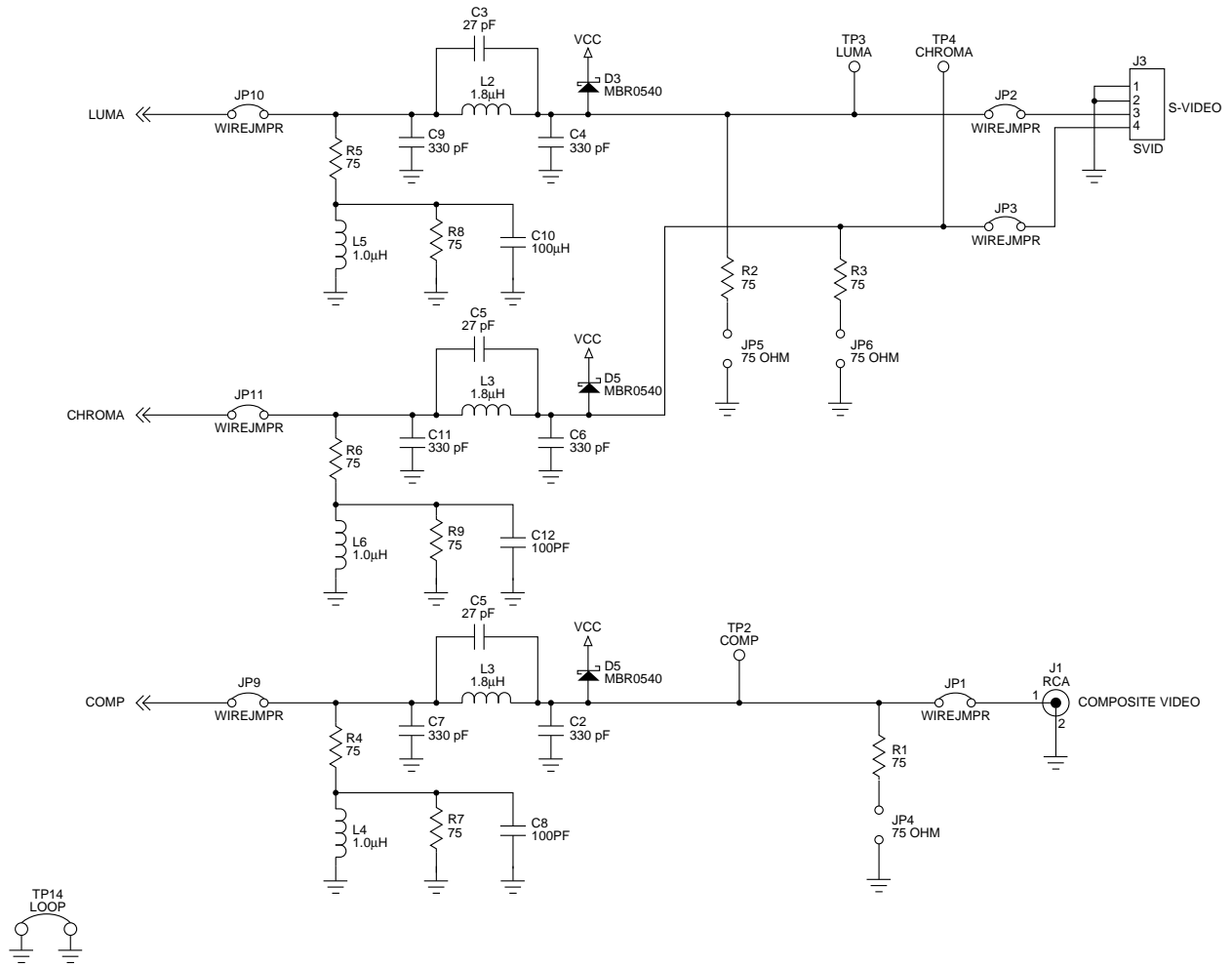


# TMC2360P7CKL Evaluation Board





### TMC2360P7CKL Evaluation Board



## Parts List

Item	Qty.	Part-Name	Reference-Designator	Description
1	2	4310R-101-473 Bourns	RN1 RN2	47K $\Omega$
2	2	RJ26FW502 Mepcopal	VR1 VR2	5K $\Omega$
3	1	RN50C49R9F	R15	50 $\Omega$ 1%
4	12	RN50C75R0F	R1 R2 R3 R4 R5 R6 R7 R8 R9 R17 R19 R21	75 $\Omega$ 1%
5	5	RN50C1000F	R16 R18 R20 R25 R28	100 $\Omega$ 1%
6	3	RN50C1500F	R22 R23 R24	150 $\Omega$ 1%
7	3	RN50C2210F	R12 R13 R14	221 $\Omega$ 1%
8	1	RN50C4750F	R10	475 $\Omega$ 1%
9	1	RN50C7500F	R11	750 $\Omega$ 1%
10	1	RN50C4751F	R32	4.75K $\Omega$ 1%
11	2	RN50C3922F	R26 R27	39.2K $\Omega$ 1%
12	3	RN50C4752F	R29 R30 R31	47.5K $\Omega$ 1%
13	3	SR151A270JAA AVX	C1 C3 C5	27 pF 5% NPO
14	3	SR151A470JAA AVX	C18 C19 C20	47 pF 5% NPO
15	3	SR151A101JAA AVX	C8 C10 C12	100 pF 5% NPO
16	6	SR151A331JAA AVX	C2 C4 C6 C7 C9 C11	330 pF 5% NPO
17	2	SR151A680JAA AVX	C13 C14	680 pF 5% NPO
18	2	SR215C104JAA AVX	C15 C16	0.1 $\mu$ F 5%
19	27	12065C104KATMA AVX	C21 C22 C23 C24 C25 C26 C27 C28 C30 C31 C32 C33 C37 C38 C39 C41 C42 C43 C44 C45 C46 C47 C48 C49	0.1 $\mu$ F
20	2	TAP226K035HSB, AVX	C17, C40	22 $\mu$ F, 35v Tantalum
21	2	TBD	C29 C36	Not Installed
22	2	TBD	C34 C35	Not Installed
23	3	IMS-2 1.8 $\mu$ H 5% Dale	L4 L5 L6	1.0 $\mu$ H 5% Shielded Inductor
24	3	IMS-2 1.0 $\mu$ H 5% Dale	L1 L2 L3	1.8 $\mu$ H 5% Shielded Inductor
25	3	MMBT2907ALT1 Motorola	Q1 Q2 Q3	General Purpose PNP
26	9	2743019447 Fair-Rite	L7 L8 L9 L10 L11 L12 L13 L14 L15	Ferrite Bead
27	1	HLMP-1640 Hewlett Packard	D1	Green LED W/ Integral Resistor
28	3	MBR0540T1 Motorola	D2 D3 D4	Shottky Diode

**Parts List** (continued)

Item	Qty.	Part-Name	Reference-Designator	Description
29	1	ACH-27.000MHz-R Abracon	Y1	TTL Clock Oscillator
30	1	HC49U FOX	Y2	27 MHz Crystal, Not Installed
31	2	AV9173-01 ICS (AVASEM)	U1 U2	PLL
32	1	TMC2360KLC Raytheon	U3	Video Output Processor
33	1	MC7805CT Motorola	U4	Voltage Regulator
34	4	320E1-1-2 (Grayx1) 320E1-1-5 (Redx1) 320E1-1-8 (Whitex2)	S1 S2 S3 S4	Push-Button Switches
35	3	BD04, C&K	S5 S6 S7	4 Position DIP Switch
36	1	617-U025S-AJ220 Amphenol	P1	25 Pin D-Type Connector, Female
37	1	748390-5, AMP	J4	15 Pin D-Type Connector, Female
38	1	749767-1, AMP	J7	15 Pin D-Type Connector, Male
39	1	749263-1, AMP	J3	S-Video Connector
40	1	16PJ097 Mouser	J1	RCA Connector
41	1	5LEA-02-1 Augat	J6	Terminal Block
42	1	5LEA-02-1 Augat	J6	Terminal Block
43	1	RAPC-722 Switchcraft	J8	Power JACK, 2.1 mm, Positive Barrel
44	1	NSH-04SB-S1-TR Robinson Nugent	J2	4 Pin Header
45	12	NSH-02SB-S1-TR Robinson Nugent	JP4 JP5 JP6 JP7 JP8 JP12 JP13 JP14 JP15 JP19 JP20 JP21	2 Pin Header
46	9	J0.100X0.125T22 Squires Electronics, Inc.	JP1 JP2 JP3 JP9 JP10 JP11 JP16 JP17 JP18	Jumper Wire
47	13	ME151-203-1000 Mouser	TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP15	Test Point
48	3	N/A	TP1 TP14 TP16	For Ground Connection, Wire Supplied By User
49	—	Not Included		
50	11	ME151-8000 Mouser	JP4-JP8, JP13-JP15, JP19- JP21	JUMPER

**Parts List** (continued)

<b>Item</b>	<b>Qty.</b>	<b>Part-Name</b>	<b>Reference-Designator</b>	<b>Description</b>
51	1	40X07680 Rev B Raytheon		Printed Wiring Board
52	4	4-40 3/8" Pan Head, Philips Screws, Stainless Steel Western Fastener		Screw
53	4	1902F Keystone		Standoff

**Notes:**

**Notes:**

**Notes:**

## Ordering Information

Product Number	TMC2360 type/mounting
TMC2360P7CKL	MQFP/soldered

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